

Exhibit 27

Paper No. 2

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS,
INC., and MICRON TECHNOLOGY TEXAS LLC,

Petitioners,

v.

NETLIST, INC.,

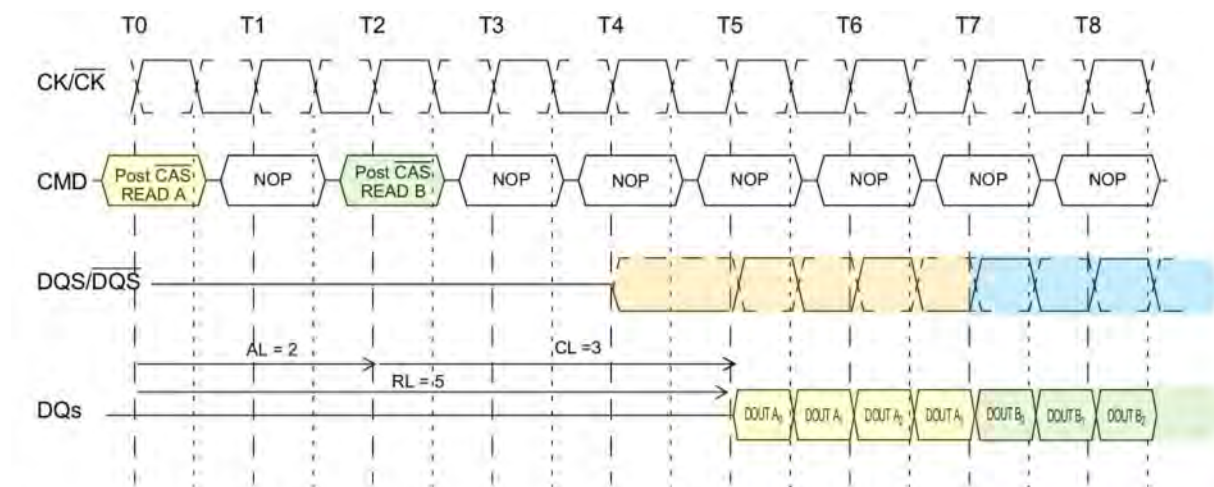
Patent Owner.

Case IPR2023-01142
Patent 9,858,215

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,858,215**

Petition for *Inter Partes* Review of U.S. Patent No. 9,858,215

strobe signals [e.g., orange DQS, at T4-T7, below] and the second burst of data strobe signals [e.g., blue DQS, at T7-, below] into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals [e.g., at T7 below, resulting in a “Seamless Burst” from the virtual rank that was created by “rank multiplication” from the first and second ranks (discussed above, pp.10-12; see also EX1071, 14:63-65, 15:37-40)].” EX1064, p.28 (below); EX1003, ¶¶478-482.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

15. Claim 14

Ground 1 teaches, as explained above for [1.d.2]-[1.d.3], [1.e.], [1.f.1]-[1.f.2] (pp.63-80), “[t]he memory module of claim 1, wherein the buffer includes circuit components [e.g., in multiplexers 530a and 530b, and interfaces 520a, 520b and 510 or 590 (and respective transceivers in those interfaces), shown below]

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configurable to provide a first data path [e.g., to interface 520a for the channel 370 to the first rank, green, below] or a second data path [e.g., to interface 520b for the channel 370 to the second rank, blue, below] depending on whether the first rank or the second rank is selected to communicate data with the memory controller.”

EX1003, ¶¶483-488.

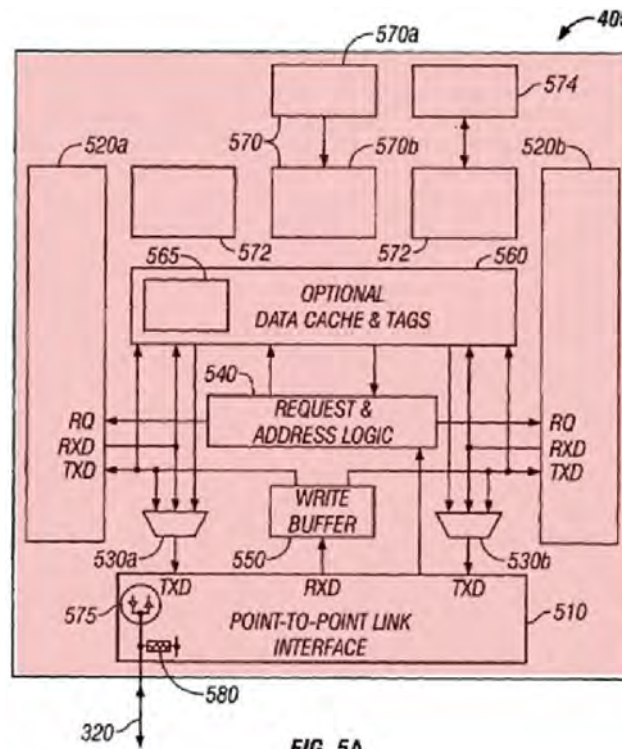


FIG. 5A

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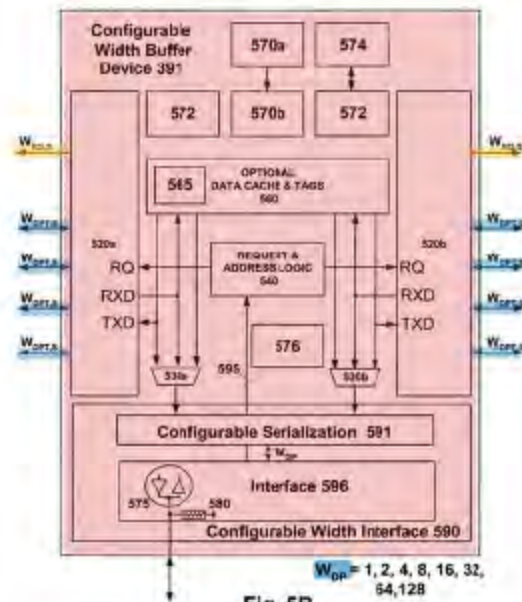


Fig. 5B

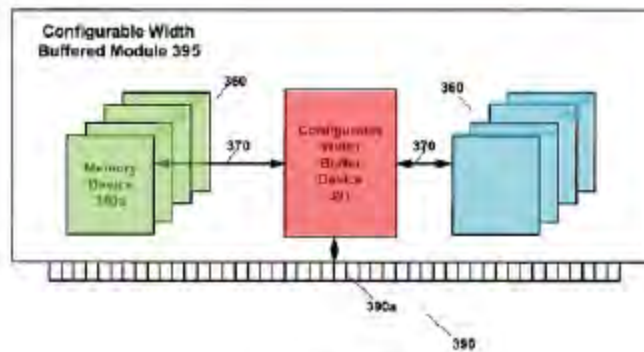


Fig. 3C

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16. Claim 15

Ground 1 teaches, as explained above for [1.d.2]-[1.d.3], [1.e.], [1.f.1]-[1.f.2] (pp.63-80), “[t]he memory module of claim 14, the^[5] at least one of the circuit components [from claim 14 (pp.107-109)] is configured to provide the first data path [from claim 14 (pp.107-109)] in response to the first control signals [from [1.f.1] (pp.76-80)], and is configured to provide the second data path [from claim 14 (pp.107-109)] in response to the second control signals [from [1.f.2] (pp.76-80)].” EX1003, ¶¶489-494.

17. Claims 16-29

The limitations of claims 16-29 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 1 for at least the same reasons discussed above:

This limitation...	...is substantially similar to this limitation...	...and thus obvious for at least the same reasons above and as discussed in EX1003:
[16]	[1.f.1], [6]	¶¶495-498 (¶¶312-324, 369-381)
[17]	[8]	¶¶499-502 (¶¶411-419)
[18]	[1.f.1], [6]	¶¶503-508 (¶¶312-324, 369-381)

⁵ This lacks antecedent basis, so this analysis assumes the claim refers to one or more “*circuit components*” from Claim 14. EX1003, ¶491.

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Dated: July 28, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. §42.24 because it contains 13,999 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. §42.24.

Dated: July 28, 2023

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CERTIFICATE OF SERVICE

I hereby certify that on this 28th day of July, 2023, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

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